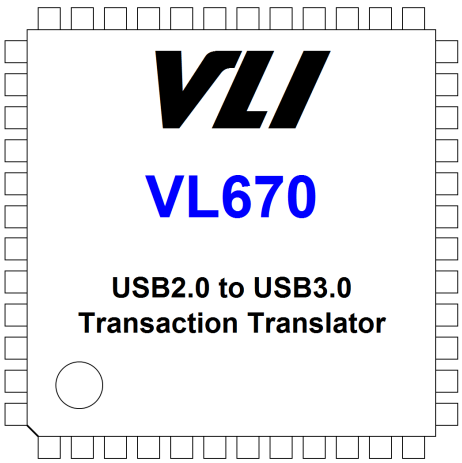
VIA Labs, Inc.

Data Sheet

VL670
USB2.0 to USB3.0
Transaction Translator

January 23, 2014
Revision 1.15



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Revision History

Rev	Date	Initial	Note
0.1	01/21/2013	HJ	Preliminary release
0.2	06/30/2013	HJ	Updated pin descriptions
0.9	08/15/2013	HJ	Updated some wordings
1.0	12/10/2013	HJ	Updated for formal release
1.1	01/15/2014	HJ	Updated top side marking information
1.15	01/23/2014	HC	Re-organized format Renamed GPIO pins Added USB electrical characteristics

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Product Features

VL670

High-Speed USB to Super-Speed USB Transaction Translator

- **Super-Speed USB (5Gb/s) and High-Speed USB (480Mb/s)**
  - Compliant to Universal Serial Bus 3.0 Specification Revision 1.0
  - Compliant to Universal Serial Bus Specification Revision 2.0
  - Support converting Bulk-Only Transport/Control/Interrupt/Isochronous type transaction between USB2.0 and USB3.0 protocol
  - Downstream port support USB 2.0 Hub
  - Integrated in-house Super-Speed USB PHY and USB2.0 PHY
- **High Performance 32-bit Microprocessor**
  - Powerful RISC processor
- **Built-in Voltage Regulators**
  - 5.0V to 3.3V LDO
  - 5.0V to 1.5V switching DC-DC
  - 1.5V to 1.2V LDO
- **GPIOs for Special Function Usage**
  - 8 GPIOs for customer special usage
  - External interrupt input x 1
  - UART interface x 1
  - SPI Slave interface x 1
- **Misc**
  - Support power saving mode
  - Support external SPI flash for firmware upgrade
  - Integrated Watch Dog
  - Integrated PLL with external 25MHz crystal
- **Physical**
  - QFN 48L green package (6x6x0.85 mm)
- **Applications**
  - Digital Signage System
  - Zero-Client
  - Industrial printer
  - Mass production system for USB products
  - HD smart video surveillance system
  - High speed data acquisition system

VL670 System Overview

VIA Lab's VL670 is the world's first and unique High-speed USB2.0 to Super-speed USB3.0 transaction translator. VL670 effectively converts USB High-speed transactions to Super-speed transactions and vice-versa. With this capability, VL670 enables USB2.0 devices to work under a USB3.0 downstream port which only provides Super-speed interface (no USB2.0 capability under this USB3.0 downstream port for specific reasons). Unlike all connected USB2.0 devices share single 480Mb/s bandwidth on the regular USB2.0 bus, the VL670-enabled USB2.0 device have whole 480Mb/s bandwidth for its own use since the upstream of VL670 has converted to the Super-speed USB transaction whose communication protocol is point-to-point based.

VL670 integrates in-house Super-speed PHY and USB 2.0 PHY and are well-tuned to provide excellent signal integrity. Both are compliant to their respective signal specification and can pass USB-IF's electrical tests as part of the certification requirements.

To provide best user experience, VL670 also provides bypass mode. When the upstream port of the VL670 is connected to an USB 2.0 downstream port, the USB 2.0 signals are bypassed from the upstream port to the downstream port directly, and vice-versa. In the case that a Super-speed capable device is attached to the downstream port of the VL670, the Super-speed signals are bypassed from the upstream to the downstream port, and vice-versa. The signal switches to enable the bypass mode are integrated in the VL670.

VL670 employs a very powerful 32-bit RISC microprocessor which allows the VL670 to quickly convert transactions/protocols between USB2.0 and USB3.0 with minimal delay. The external SPI ROM provides the flexibility for future firmware update and customization. GPIO pins, UART interface, SPI slave interface, watch-dog timer, and external interrupt are also supported to satisfy the requirements for different applications. VL670 works perfectly with a single power input from USB 5V bus to save customer BOM cost and is available on QFN 64L green package (6x6x0.85 mm).

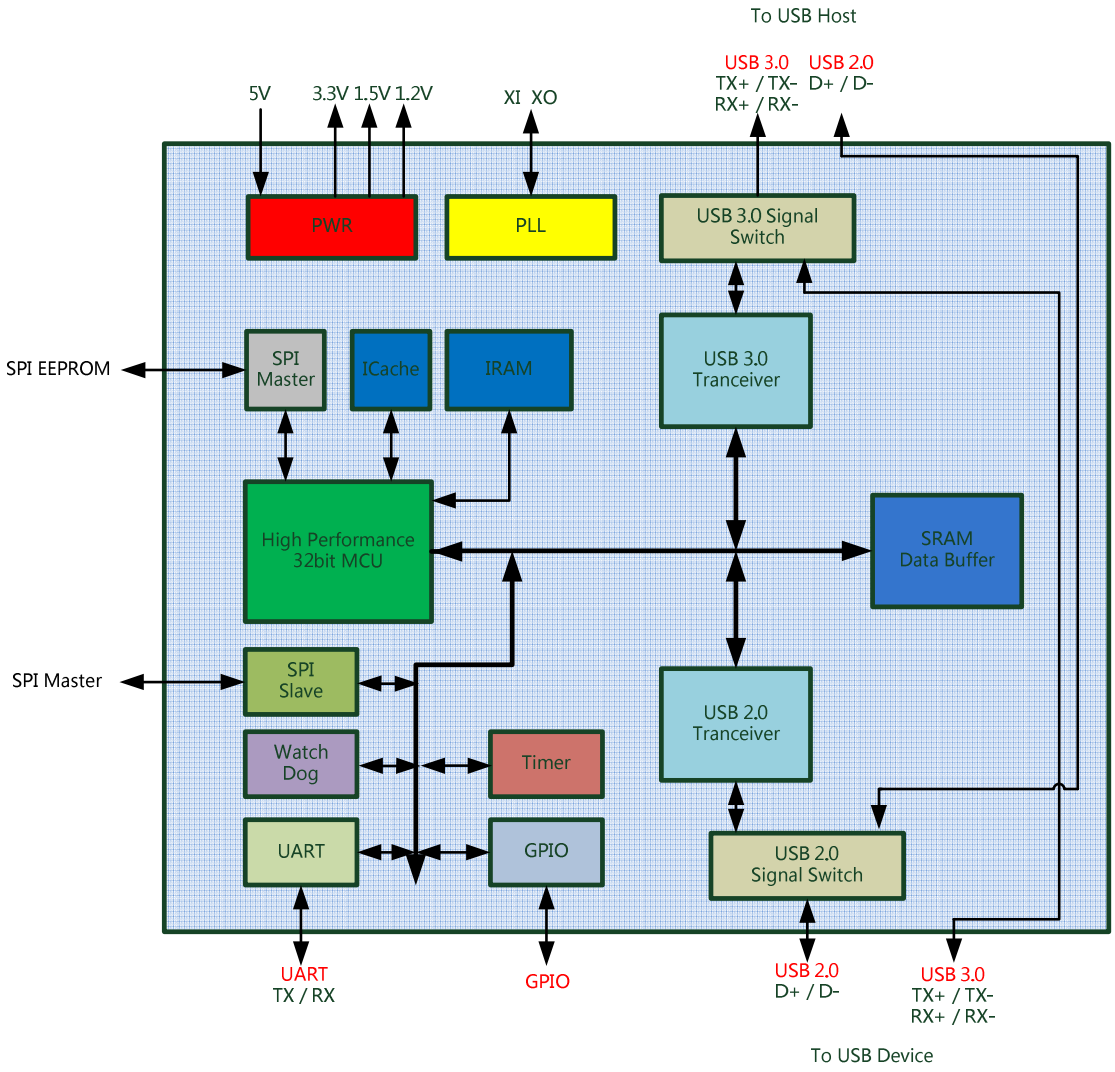


Figure 1 – VL670 Block Diagram

Typical Applications

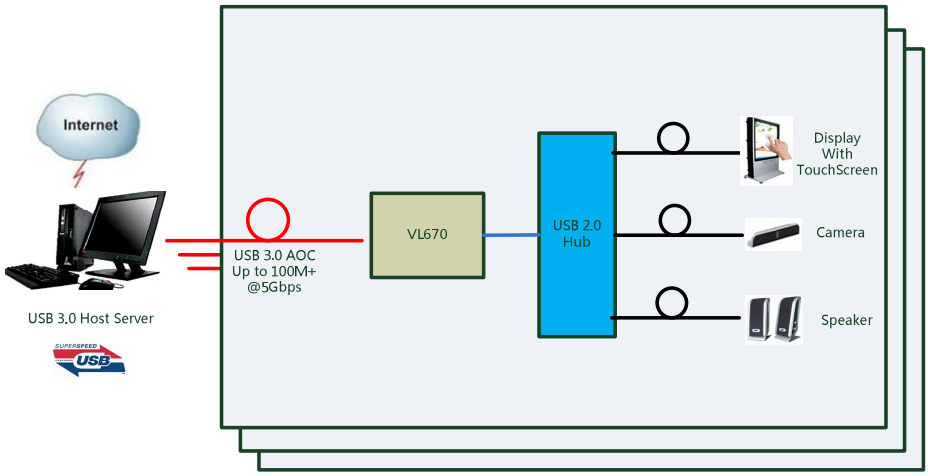


Figure 2 – Digital Signage System with VL670

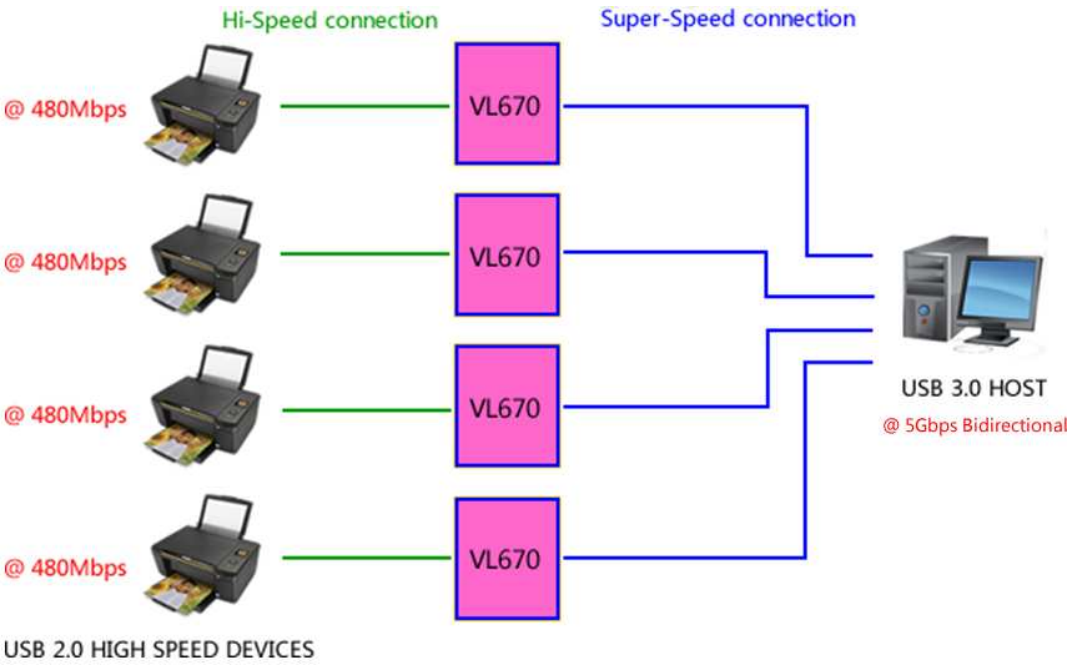


Figure 3 – High speed industrial printers with VL670

Pinout

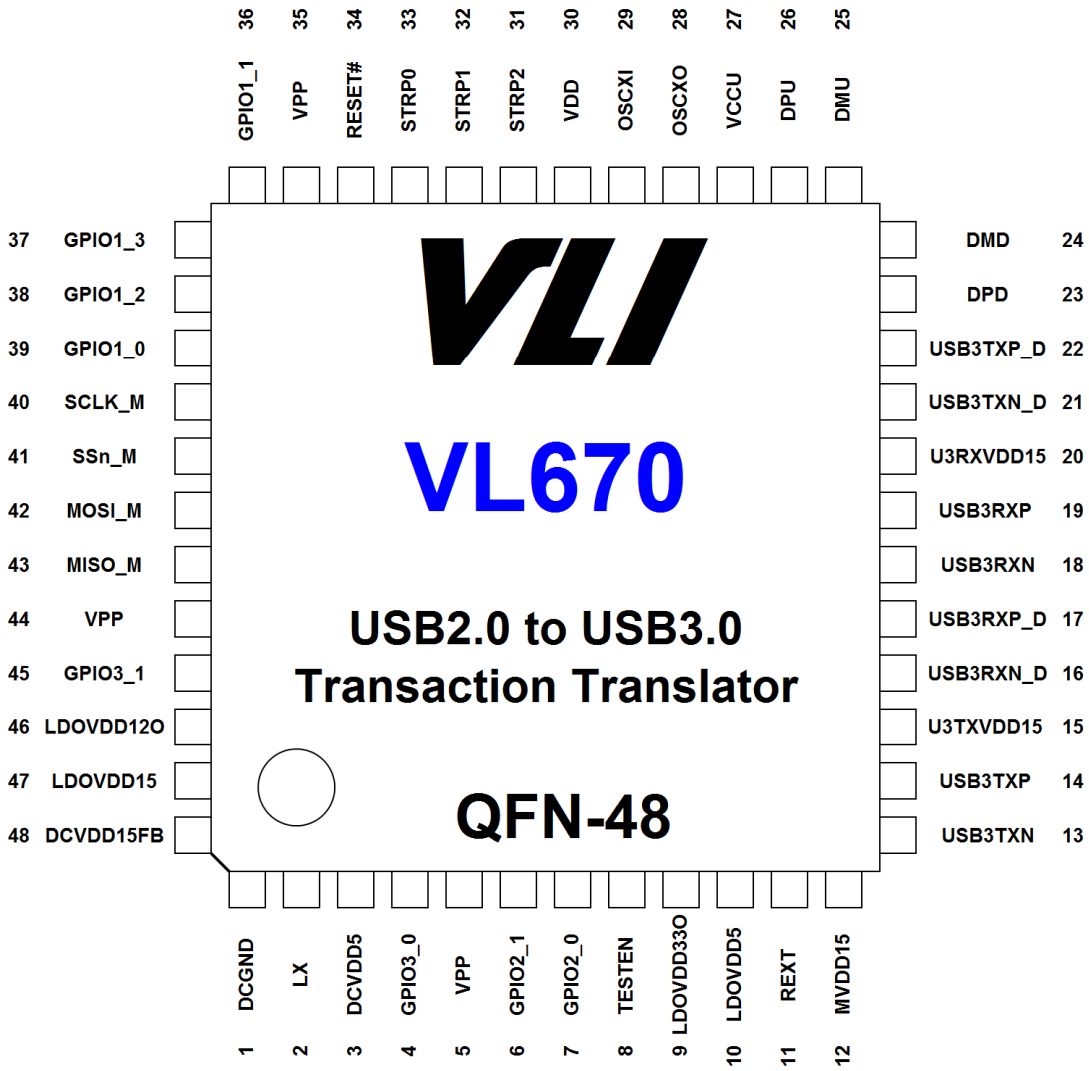


Figure 4 – VL670 QFN-48 Pin Diagram

Pin List

Table 1 – VL670 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	DCGND	25	DMU
2	LX	26	DPU
3	DCVDD5	27	VCCU
4	GPIO3_0	28	OSCXO
5	VPP	29	OSCXI
6	GPIO2_1	30	VDD
7	GPIO2_0	31	STRP2
8	TESTEN	32	STRP1
9	LDOVDD33O	33	STRP0
10	LDOVDD5	34	RESET#
11	REXT	35	VPP
12	MVDD15	36	GPIO1_1
13	USB3TXN	37	GPIO1_3
14	USB3TXP	38	GPIO1_2
15	U3TXVDD15	39	GPIO1_0
16	USB3RXN_D	40	SCLK_M
17	USB3RXP_D	41	SSn_M
18	USB3RXN	42	MOSI_M
19	USB3RXP	43	MISO_M
20	U3RXVDD15	44	VPP
21	USB3TXN_D	45	GPIO3_1
22	USB3TXP_D	46	LDOVDD12O
23	DPD	47	LDOVDD15
24	DMD	48	DCVDD15FB

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

Upstream USB Interface

Pin Name	Pin #	I/O	Signal Description
USB3TXN	13	O	USB 3.0 Differential Transmit Data-
USB3TXP	14	O	USB 3.0 Differential Transmit Data+
U3TXVDD15	15	PWR	Analog 1.5V Power
USB3RXN	18	I	USB 3.0 Differential Receive Data-
USB3RXP	19	I	USB 3.0 Differential Receive Data+
USB3RXVDD15	20	PWR	Analog 1.5V Power
DMU	25	I/O	USB 2.0 Bus Data Minus(D-)
DPU	26	I/O	USB 2.0 Bus Data Plus(D+)

Downstream USB Interface

Pin Name	Pin #	I/O	Signal Description
USB3TXN_D	21	O	USB 3.0 Differential Transmit Data-
USB3TXP_D	22	O	USB 3.0 Differential Transmit Data+
USB3RXN_D	16	I	USB 3.0 Differential Receive Data-
USB3RXP_D	17	I	USB 3.0 Differential Receive Data+
DMD	24	I/O	USB 2.0 Bus Data Minus(D-)
DPD	23	I/O	USB 2.0 Bus Data Plus(D+)
VCCU	27	PWR	Analog 3.3V Power

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
OSCXO	28	O	25M crystal output
OSCXI	29	I	25M crystal input
REXT	11	A_{BIAS}	USB 3.0 reference resistor

Serial EEPROM Interface

Pin Name	Pin #	I/O	Signal Description
SCLK_M	40	O	Clock for SPI Master; Serial Flash Clock
SSn_M	41	O	Chip select for SPI Master; Serial Flash Chip Enable
MOSI_M	42	O	MOSI for SPI Master; Serial Flash Data Input

MISO_M	43	I	MISO for SPI Master; Serial Flash Data Output

General Purpose I/O and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
RESET#	34	I	External Chip Reset
STRP0	33	I	Mode setting pin 0
STRP1	32	I	Mode setting pin 1
STRP2	31	I	Mode setting pin 2
GPIO1_0	39	I/O	General purpose input output pin Default: SCLK for SPI Slave External interrupt, high active
GPIO1_1	36	I/O	General purpose input output pin Default: Chip select for SPI slave
GPIO1_2	38	I/O	General purpose input output pin Default: MOSI for SPI Slave
GPIO1_3	37	I/O	General purpose input output pin Default: MISO for SPI Slave
GPIO2_1	6	I/O	General purpose input output pin Default: TX of UART
GPIO2_0	7	I/O	General purpose input output pin Default: RX of UART
GPIO3_0	4	I/O	General purpose input output pin
GPIO3_1	45	I/O	General purpose input output pin

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	8	I	Test Mode Enable

Power and Ground

Pin Name	Pin #	I/O	Signal Description
DCGND	1	GND	Ground for internal DC-DC regulator
LX	2	O	1.5V voltage output for internal DC-DC regulator
DCVDD5	3	PWR	5.0V voltage input for internal DC-DC regulator
VPP	5,35,44	PWR	3.3V IO power
LDOVDD33O	9	O	3.3V voltage output for 5V to 3.3V LDO
LDOVDD5	10	PWR	5.0V voltage input for 5V to 3.3V LDO
MVDD15	12	PWR	1.5V Master analog power
VDD	30	PWR	1.2V Core power
LDOVDD12O	46	O	1.2V voltage output for 1.5V to 1.2V LDO
LDOVDD15	47	PWR	1.5V voltage input for 1.5V to 1.2V LDO
DCVDD15FB	48	I	1.5V feedback for internal DC-DC regulator

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW code for VL670. Timing guidelines are provided to assist selecting appropriate and compatible SPI flash. To make sure the selected SPI flash is compatible, not only should the timing requirements conform to the provided guidelines, but actual testing with VL670 should also be done. Note that the clock frequency for read cannot be less than 20MHz.

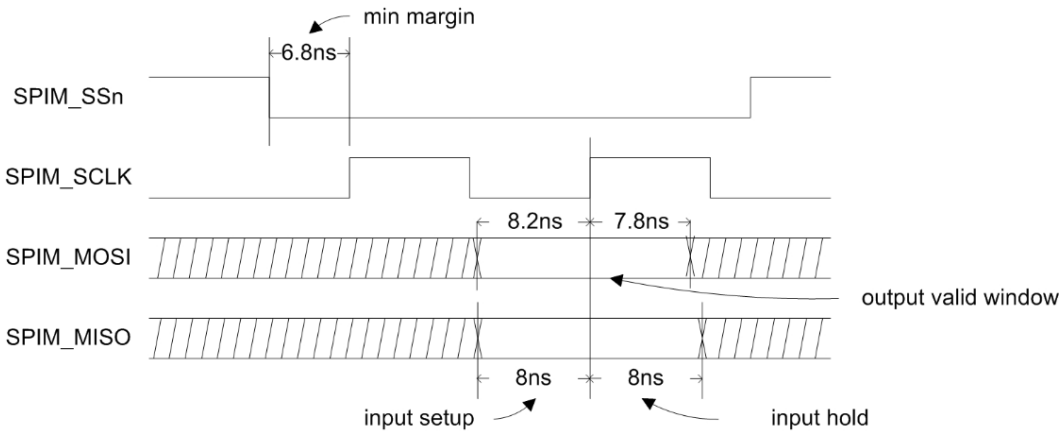


Figure 5 – SPI Flash timing requirement

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
DCVDD5	Power Supply Voltage of 5V to 1.5V DC-DC	-0.3	5.5	V	—
LDOVDD5	Power Supply Voltage of 5V to 3.3V LDO	-0.3	5.5	V	—
V_{IN}	Input Voltage at I/O pins	-0.3	3.63	V	—
V_{ESD}	Electrostatic Discharge	—	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient Temperature	0	25	70	°C
DCVDD5	Power Supply Voltage of 5V to 1.5V DC-DC	4.75	5	5.25	V
LDOVDD5	Power Supply Voltage of 5V to 3.3V LDO	4.75	5	5.25	V
DCGND	Ground	—	0	—	V
I_C	Power consumption	Active mode: 150 Power Saving mode: 100 Suspend mode: 10			mA

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	—	0.4	V	—
V_{IH}	Input High Voltage	2.0	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=-4.0mA
V_{OH}	Output High Voltage	2.0	—	V	IOH=4.0mA

USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{FSIH}	Full-speed Input High	2.0		V	—
V_{FSIL}	Full-speed Input Low		0.8	V	—
V_{FSCM}	Differential Common Mode Voltage	0.8	2.5	V	—
V_{FSOL}	Full-speed Output Low	0.0	0.3	V	—
V_{FSOH}	Full-speed Output High	2.8	3.6	V	—
T_{FSR}	Full-speed Rise Time	4	20	ns	—
T_{FSF}	Full-speed Fall Time	4	20	ns	—
V_{FSCRS}	Full-speed Output Signal Crossover Voltage	1.3	2.0	V	—

USB High Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{HSSQ}	High-speed squelch detection threshold	100	150	mV	—
V_{HSCM}	High-speed data signaling common mode voltage	-50	500	mV	—
V_{HSOI}	High-speed idle level	-10	10	mV	—
V_{HSOH}	High-speed data high	360	440	mV	—
V_{HSOL}	High-speed data low	-10	10	mV	—
V_{CHIRPJ}	Chirp J level	700	1100	mV	—
V_{CHIRPK}	Chirp K level	-900	-500	mV	—
Z_{HSDRV}	Drive output resistance	40.5	49.5	Ω	—
T_{HSR}	High-speed Rise Time	500		ps	—
T_{HSF}	High-speed Fall Time	500		ps	—

USB Super Speed TX Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{TX-DIFF-PP}$	Differential p-p Tx swing	0.8	1.2	V	—
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0	4.0	dB	—
$R_{TX-DIFF-DC}$	DC differential impedance	72	120	Ω	—
$V_{TX-RCV-DETECT}$	The Voltage Change allowed during Receiver Detection		0.6	V	—
T_{TX-EYE}	Transmitter Eye	0.625		UI	—
$T_{TX-DJ-DD}$	Tx Deterministic Jitter		0.205	UI	—
R_{TX-DC}	Transmitter DC Common Mode Impedance	18	30	Ω	—
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0	2.2	V	—
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC Common Mode Voltage Active		100	mV	—
$V_{TX-IDLE-DIFF-AC-pp}$	Electrical Idle Differential P-P Output Voltage	0	10	mV	—
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0	10	mV	—

USB Super Speed RX Characteristics (5.0 GT/s)

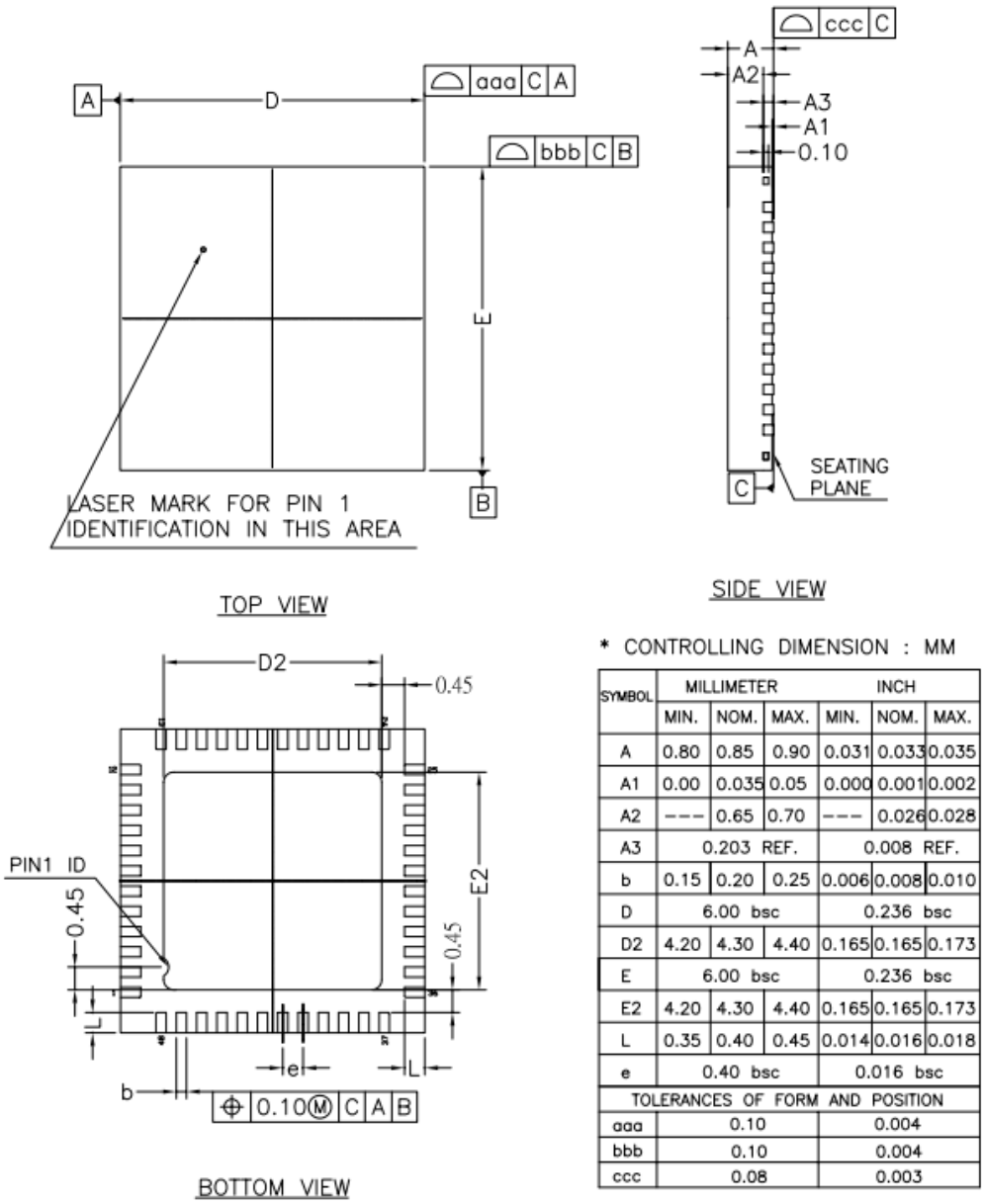
Symbol	Parameter	Min	Max	Unit	Note
UI	Unit Interval	199.94	200.06	ps	UI does not account for SSC caused variations
R_{RX-DC}	Receiver DC common mode impedance	18	30	Ω	DC impedance limits are needed to guarantee Receiver detect Measured with respect to ground over a voltage of 500mV maximum
$R_{RX-DIFF-DC}$	DC differential impedance	72	120	Ω	

$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25k		Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500mv with respect to ground
$V_{RX-LFPS-DET-DIFF_{p-p}}$	LFPS Detect Threshold	100	300	mV	Below the minimum is noise Must wake up above the maximum
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30		mV	Measured after the Rx EQ function (Section 6.8.2)
t_{RX-TJ}	Max Rx inherent timing error		0.45	UI	Measured after the Rx EQ function (Section 6.8.2)
$t_{RX-DJ-DD}$	Max Rx inherent deterministic timing error		0.3	UI	Maximum Rx inherent deterministic timing error
$C_{RX-PARASITIC}$	Rx input capacitance for return loss		1.1	pf	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage		150	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$	Rx AC common mode voltage during the U1 to U0 transition		200	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz

Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D2	4.20	4.30	4.40	0.165	0.165	0.173
E	6.00 bsc			0.236 bsc		
E2	4.20	4.30	4.40	0.165	0.165	0.173
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.08			0.003		

Figure 6 – QFN 48L 6x6x0.85 mm Mechanical Specification

Package Top Side Marking & Ordering Information

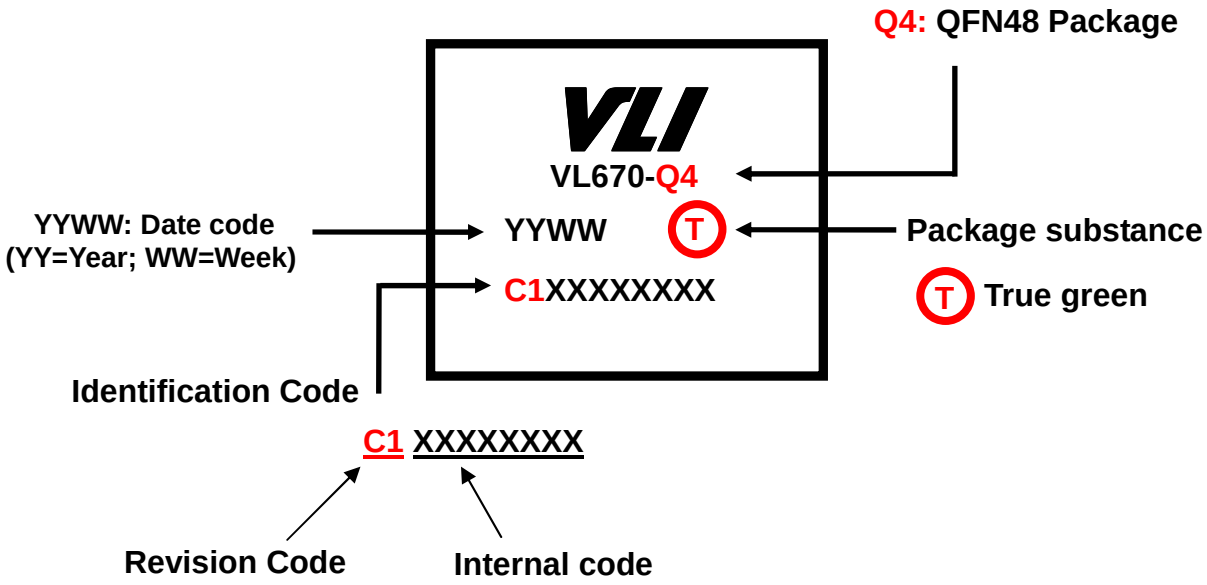


Figure 7 – VL670 Package Top Side Marking

Part Number	Description	Package
VL670-Q4	Standard configuration	48-pin QFN (6x6mm)

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